WHAT IS CLAIMED is:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a first insulation layer formed on an inner surface of a trench formed in the semiconductor substrate and having its top located above the surface of the semiconductor substrate;

a diffusion layer formed within the semiconductor substrate, surrounding the deep portion of the trench;

a first conductive layer filled in the trench;

a gate electrode provided on a gate insulation layer formed on the surface of the semiconductor substrate;

source/drain diffusion layers formed in the surface of the semiconductor substrate, sandwiching a channel region below the gate electrode; and

a second conductive layer extending on the first conductive layer, the first insulation layer, and one of the source/drain diffusion layers.

2. The device according to claim 1, wherein the first insulation layer is provided on the inner surface of the trench without exposing a side of the semiconductor substrate within the trench.

3. The device according to claim 2, wherein the second conductive layer is provided without contacting the side of the semiconductor substrate.

4. The device according to claim 1, wherein a top

of the first conductive layer is located above the surface of the semiconductor substrate.

5. The device according to claim 1, further comprising a second insulation layer overlying the top of the first insulation layer.

6. The device according to claim 1, further comprising a third insulation layer provided on the first conductive layer and consisting of a same material of the first insulation layer.

7. The device according to claim 6, further comprising a device isolation insulation layer consisting of a same material as the first and third insulation layers and having in its surface a concave whose bottom is located above the surface of the semiconductor substrate.

8. A method of manufacturing a semiconductor memory device comprising:

forming a capacitor in a trench formed in a semiconductor substrate, the capacitor having a first dielectric layer whose top is at a first level above the surface of the semiconductor substrate and a first conductive layer which fills the trench;

forming a second insulation layer on the first insulation layer and the first conductive layer in an upper portion of the trench;

forming a transistor on the semiconductor substrate, the transistor having a gate electrode and

source/drain diffusion layers formed in the surface of the semiconductor substrate, the source/drain diffusion layers sandwiching a channel region below the gate electrode;

removing a portion of the second insulation layer to expose a top of the first conductive layer; and

forming a connecting conductive layer on the exposed first conductive layer and one of the source/drain diffusion layers.

9. The method according to claim 8, wherein forming the capacitor includes

forming a third insulation layer on the semiconductor substrate;

forming the trench in the third insulation layer and the semiconductor substrate;

forming the first insulation layer on an inner surface of the trench;

forming the first conductive layer in the trench, a top of the first conductive layer being located above the surface of the semiconductor substrate, and

removing the third insulation layer.

10. The method according to claim 9, wherein forming the second insulation layer includes filling an upper portion of the trench with the second insulation layer prior to removal of the third insulation layer.

11. The method according to claim 10, wherein the first insulation layer is formed on the inner surface

of the trench without exposing a sidewall of the semiconductor substrate within the trench.

12. The method according to claim 11, wherein removing a portion of the second insulation layer includes lowering a top of the first insulation layer from the first level to a second level, and

the first level is set so that the second level is above the semiconductor substrate surface level.

13. The method according to claim 8, further comprising, prior to forming the connecting conductive layer, forming a fourth insulation layer on that surface of the first insulation layer which is above the surface of the semiconductor substrate.

14. The method according to claim 13, wherein forming the fourth insulation layer includes forming a fifth insulation layer on the sidewall of the gate electrode.

15. The method according to claim 8, further comprising;

prior to formation of the transistor, forming a device isolation insulation layer in a position where a portion of each of the semiconductor substrate, the capacitor, and the second insulation layer has been removed, and

after formation of the transistor, forming an interlayer insulation layer on the device isolation insulation layer, the second insulation layer, and the

source/drain diffusion layers;

removing the interlayer insulation layer on the second insulation layer and the source/drain diffusion layers, and

wherein forming the connecting conductive layer includes forming the connecting conductive extending on the exposed first conductive layer and one of the source/drain diffusion layers.

16. The method according to claim 8, further comprising, prior to formation of the transistor, forming a device isolation insulation layer in a position where a portion of each of the semiconductor substrate, the capacitor, and the second insulation layer has been removed, and

wherein forming the connecting conductive layer includes

forming the connecting conductive layer on the exposed first conductive layer, the source/drain diffusion layers, and the device isolation insulation layer and

removing the connecting conductive layer on the device isolation insulation layer.

17. The method according to claim 8, wherein forming the connecting conductive layer includes epitaxially growing a crystal as the connecting conductive layer from the semiconductor substrate.

18. The method according to claim 8, wherein

forming the connecting conductive layer includes

depositing a second conductive layer that forms the connecting conductive layer on an area where the connecting conductive layer is to be formed and

causing a top of the second conductive layer to retreat.